50. (New) The field emitter array of claim 47, wherein the number of gate lines include doped polysilicon.

51. (New) A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes;

wherein the number of cathodes include metal silicides on the polysilicon cones.

52. (New) A field emitter array, comprising:

a number of cathodes in rows along a semiconductor-on-glass substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

53. (New) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes; and

a row decoder and a column decoder each coupled to the field emitter array; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

54. (New) The flat panel display of claim 53, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

55. (New) The flat panel display of claim 53, wherein the number of cathodes include metal silicides on the polysilicon cones.

56. (New) The flat panel display of claim 53, wherein the number of gate lines include refractory metals.

57. (New) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness ;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels; and

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.